UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
TYLER DIVISION

Stragent, LLC, *Plaintiff*, v. Intel Corporation, *Defendant*.	Case No. 6:11-cv-421

SUPPLEMENTAL CLAIM CONSTRUCTION OPINION

On March 6, 2014, the court issued a supplemental claim construction order addressing the meaning of four terms of U.S. Patent Nos. 6,848,072 (the '072 patent) and 7,028,244 (the '244 patent) that were relevant to the case. Suppl. Claim Constr. Order, March 6, 2014, ECF No. 294. The order instructed that "[a] written opinion explaining the court's reasons for adopting these claim constructions will issue in due course." *Id.* at 1. This is that opinion.

DISCUSSION

The Federal Circuit's principles for claim construction are established by *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–19 (Fed. Cir. 2005) (en banc), and subsequent decisions. The supplemental claim constructions here were based on the parties' briefs, Def.'s Suppl. Claim Constr. Br., Feb. 28, 2014, ECF No. 278; Pl.'s Resp., March 4, 2014, ECF No. 281, and the oral arguments presented at the supplemental claim construction hearing on March 6, 2014. At the hearing, the court proposed language for the four supplemental constructions and entertained the parties' suggestions and objections to those proposals. Only the first and second proposed constructions drew objections; the third and fourth were accepted by both parties. Suppl. Claim

Constr. Hr'g Tr. 75–78, March 7, 2014, ECF No. 290. Accordingly, this opinion will address only the first and second supplemental claim constructions in the supplemental claim construction order.

1. "a first Cyclic Redundancy Check (CRC) circuit" and "a second CRC circuit"; "a plurality of CRC circuits"

Two of the asserted claims in this case call for a device and a method comprising multiple CRC circuits, each with its own hardwired CRC polynomial. Claim 12 of the '072 patent recites a device comprising "a first Cyclic Redundancy Check (CRC) circuit configured to perform a first CRC operation" and "a second CRC circuit configured to perform a second CRC operation" having a "first polynomial" and "second polynomial," respectively, hardwired into each circuit. '072 patent col. 6 l. 63, col. 7 l. 1. Similarly, claim 1 of the '244 patent recites a method comprising "a plurality of CRC circuits . . . each . . . including a CRC polynomial hardwired therein." '244 patent col. 6 l. 11. The court construed the "first" and "second" CRC circuits in '072 patent claim 12 and the "plurality" of CRC circuits in '244 patent claim 1 to be "separate circuits that do not share an output register or feedback paths." Stragent had no objection to the court's construction. Intel objected.

Intel agreed that the circuits in both claims must be separate, but argued that there was no reason that separate circuits could not share output registers or feedback paths. In Intel's view, the separate circuits are simply "circuits that have independent hardwired polynomials . . . [a]nd there is no other requirement that should be imported into the meaning of the [claims]." Suppl. Claim Constr. Hr'g Tr. 76.

Intel's position—that, to be "separate," circuits need only have separate hardwired polynomials—is belied by the patent. Both the specification and claims contemplate a single

CRC circuit having more than one hardwired CRC polynomial. *See* '072 patent col. 5 ll. 37–44 ("Multiple CRC operations, each potentially using a different polynomial, may be implemented in separate CRC circuits. . . . In alternate implementations, instead of using four separate CRC circuits 305–308 [referring to figure 3 of the patent], *a single CRC circuit could be used that includes four separate hardwired polynomials*." (emphasis added)); *id.* col. 6. ll. 36–38 ("one CRC circuit for generating a CRC result based on hardwired CRC polynomials"). The fact that a single CRC circuit may have multiple hardwired polynomials means that separate polynomials are not enough by themselves to make separate circuits.

Separateness necessarily implies that the CRC circuits of the claims can function separately. The claims do not require that the circuits both be able to operate simultaneously, but they do appear to require independent operation. Claim 12 of the '072 patent requires that each circuit be "configured to perform a . . . CRC operation." '072 patent col. 6 ll. 62–63, col. 7. ll. 1–2. This implies that each circuit must have sufficient components to perform a CRC operation on its own. While neither the specification nor the claims addresses the sharing of feedback paths or output registers, the parties agreed that those components are necessary to the functioning of a CRC circuit in common applications. Thus, in order to function separately, as the claims imply that they must, the separate CRC circuits cannot share feedback paths or output registers.

Nothing in the specification or claims is to the contrary. Intel argues that Figure 3 from the patent, depicted below, supports its position. The figure shows a device comprising four separate CRC circuits. Also shown are various links between the circuits and the outside world, such as the input and output buses. Intel contends that the highlighted portions of Figure 3 show feedback paths and an output register that are shared between the separate CRC circuits. But the patent nowhere describes the highlighted portions as feedback paths or output registers. Rather,

they simply show the input and output buses to be used by the CRC circuits as a whole. The feedback paths and output registers are not depicted in Figure 3.

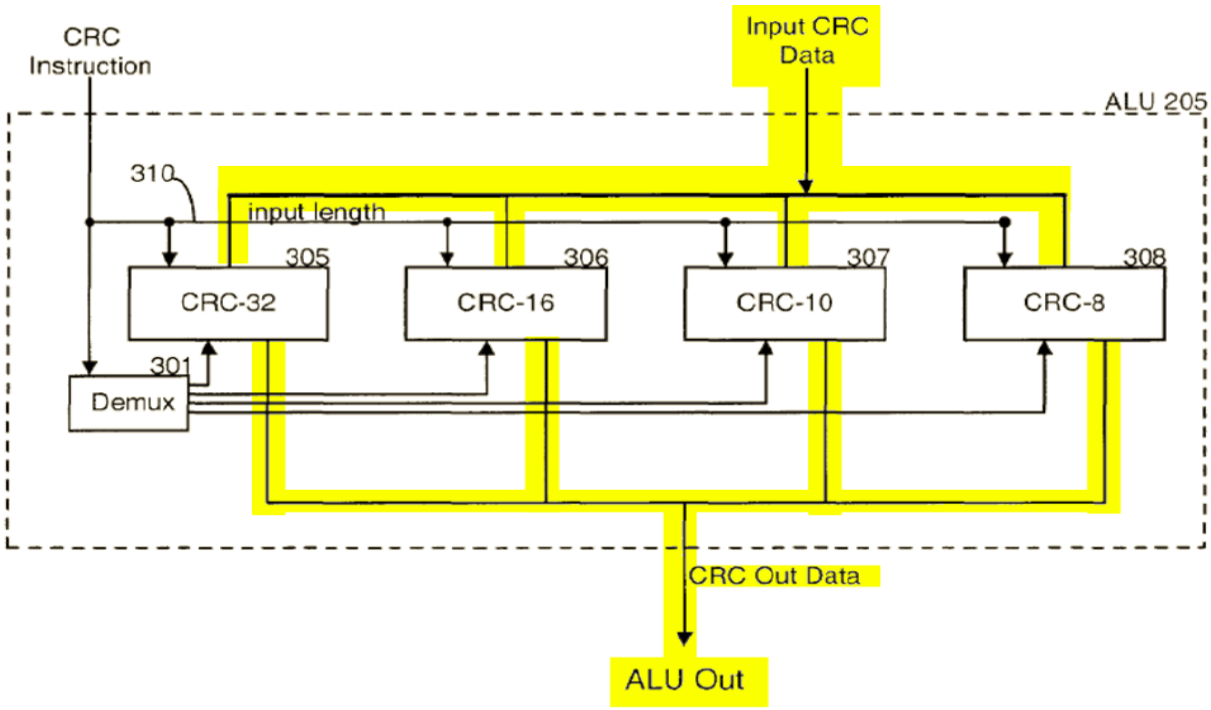

Figure 3 from the ’072 patent specification.

Intel also relies on the provisional application that preceded the ’072 and ’244 patents. The court does not find the provisional application useful, as it does not require two or more separate circuits. Stragent no longer claims that the patents are entitled to the priority date of the provisional application.

This issue presents a close question because the specification provides no real guidance. On balance, the court concludes that Stragent’s position more naturally aligns with the language of the claims.

2. “CRC output result”; “CRC result”

The second disputed claim construction concerns the “CRC result” or “CRC output result” that is calculated by the CRC circuits using the hardwired polynomials. Claim 12 of the ’072 patent recites that each CRC circuit is “configured to perform a . . . CRC operation on the

input data" and that whichever circuit is used at a given time will "generate a CRC output result based on the input data." '072 patent col. 6 ll. 62–63, col. 7 ll. 1–2, 11. Claim 1 of the '244 patent similarly recites that input data will be received "at the selected CRC circuit" which will "generat[e] the CRC result." '244 patent col. 6 ll. 15–16. The court construed "CRC output result" and "CRC result" as "value equal to the complete remainder of the input data divided by a CRC polynomial, but not a partial remainder or interim result that is carried forward for use in a successive operation of the same circuit."

Stragent again had no objection to the court's construction. But Intel objected. Prior to the supplemental claim construction, the court had previously construed the CRC result claim terms to mean "a value equal to the remainder of the input data divided by the CRC polynomial." At the claim construction hearing it became apparent that the parties had a disagreement as to the CRC result terms.

In many implementations of a CRC circuit, the processor will be asked to calculate a single CRC value for a packet of data that has more bits than the processor can take in at once. To use a simple example, a 32-bit processor—that is, a processor capable of processing 32 bits at a time—may be asked to calculate a CRC value for a string of data that is 128 bits long. In that case, the processor must divide each 32-bit chunk by the CRC polynomial and carry forward the interim remainder for use in the division of the next 32-bit chunk by the CRC polynomial. This process must be repeated (four times in the example here) to reach the final result that will be concatenated (appended) to the input data for use in error checking.[1]

[1] In a sense, this process is much like the one used to do long division. At each step, part of the number to be divided (the dividend) is divided by the divisor and the partial remainder is carried forward into the next division step. The process is performed as many times as necessary to reach the final result.

Intel's position is that each interim remainder that is carried forward to the next iteration of the process (sometimes called a residue) is a CRC result within the meaning of the claims. As Intel explained at the hearing, each residue "is the polynomial divided into the data that was put into the circuit." Suppl. Claim Constr. H'rg Tr. 17. Stragent's position is that only the final result is a CRC result.

The specification supports Stragent's position. Although it does not explicitly define the CRC result, the specification in several places refers to the CRC result as the value that is concatenated to the input data for use in error checking. For example, in describing the basic process of CRC error checking, the specification states:

> The CRC result can be sent or stored along with the original data. When the data is received (or recovered from storage) the CRC operation can be reapplied, and the latest result compared to the original result. If no error has occurred, the CRC results should [] match.

'072 patent col. 3 ll. 64–65. Later, in discussing exemplary Figure 4, the specification refers to the result reached at the end of an iterative process as the CRC result: "After the last bit is input to logic gate 422, the resultant value stored in registers 410–414 is the CRC result value (i.e., 01110). In this implementation, the total input value is a 20 bit number, and accordingly, CRC calculation circuit 400 may process this number in 20 clock cycles." *Id.* col. 5. ll. 18–22. Other portions of the specification support Stragent's reading as well. *See id.* col. 5 ll. 23–26 ("When checking the input data portion 31 based on a previously calculated CRC result value, network processor 200 concatenates the input data portion 431 with the previous CRC result value . . . ."); *id.* col 5. ll. 31–34 ("When using a CRC circuit to subsequently check the integrity of the data, the data is concatenated with the CRC result value and input to the CRC circuit 400. If there are no errors in the data value, the new CRC result should be zero.").

On balance, the court concludes that Stragent's position more naturally aligns with the claim language and the specification.

3. "input data"

Both claim 12 of the '072 patent and claim 1 of the '244 patent call for CRC operations to be performed on "input data." '072 patent col. 6 l. 64, col. 7 ll. 2, 11; '244 patent col. 6 ll. 6, 16. The court construed "input data" to be "the block of data equivalent in size to the processor capacity (*e.g.*, 32 bits for a 32-bit processor)—but not necessarily an entire data packet—from which a complete CRC result is to be calculated by performing a CRC operation." Neither party objected to this construction.

4. "parallel decomposition of a serial CRC circuit"

Claim 16 of the '072 patent, which depends from claim 12 of the same patent, recites a device wherein the first and second CRC circuits comprise "exclusive-or gates configured as a parallel decomposition of a serial CRC calculation circuit." '072 patent col. 7 ll. 26-27. The court construed the "parallel decomposition of a serial CRC circuit" to be a "circuit that calculates a CRC result by processing all bits of the input data at one time, instead of a lesser number of bits such as two." Neither party objected to this construction.

Signed April 7, 2014.

Hon. Timothy B. Dyk
United States Circuit Judge*

* Of the United States Court of Appeals for the Federal Circuit, sitting by designation.